AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A real time control system of a multitasking digital signal processor, comprising:

a ready queue ~~including~~ comprising:

a ready queue link, the ready queue link comprising ~~a~~ first information indicating a first task control block for a sequentially first task among tasks in the digital signal processor, and a second task control block for a sequentially last task among the tasks in the digital signal processor, and

a first priority link group of first priority links, a number of the first priority links being equal to a number of priority levels of the tasks in the digital signal processor, ~~and~~each of said first priority links having ~~a~~ second information indicating a third task control block for a sequentially first task among respective tasks having a same priority as each of said first priority links, among the tasks in the digital signal processor, and a fourth task control block for a sequentially last task among the respective tasks having the same priority as each of said first priority links;

and

an operating system for setting the first and second information according to conditions of the tasks ~~for~~ in the digital signal processor, and controlling switching between ~~the~~ tasks of the ready queue.

2. (currently amended): The real time control system of claim 1, wherein the first information comprises a first ~~list~~ pointer corresponding to the first task control block and a second pointer corresponding to the second task control block, and

the second information comprises a third ~~list~~ pointer corresponding to the third task control block and a fourth pointer corresponding to the fourth task control block.

3. (currently amended): The real time control system of claim 1, wherein the operating system updates the first and second information so that deterministic scheduling with respect to the ready queue link and the first priority links is maintained, when a task for the digital signal processor is inserted or deleted.

4. (currently amended): The real time control system of claim 1, further comprising a waiting queue, the waiting queue including:

a waiting queue link~~, the waiting queue link~~ comprising ~~a~~ third information indicating ~~a fifth~~ the first task control block for the sequentially first task among the tasks in the digital signal processor, and ~~a sixth~~ the second task control block for the sequentially last task among the tasks in the digital signal processor, and

a second priority link group of second priority links, a number of the second priority links being equal to the number of priority levels of the tasks in the digital signal processor, ~~and~~each of said second priority links having ~~a~~ fourth information indicating ~~a seventh~~ the third task control block for the sequentially first task among the respective tasks having the same priority as each of said second priority links, among the tasks in the digital signal processor, and ~~an eighth~~ the fourth task control block for the sequentially last task among the respective tasks having the same priority as each of said second priority links,

wherein the operating system sets the third and fourth information so that resources for ~~the~~ tasks of the waiting queue are deterministically acquired.

5. (currently amended): The real time control system of claim 4, wherein the third information comprises a fifth ~~list~~ pointer corresponding to the ~~fifth~~ first task control block and a sixth pointer corresponding to the ~~sixth~~ second task control block, and

the fourth information comprises a seventh ~~list~~ pointer corresponding to the ~~seventh~~ third task control block and an eighth pointer corresponding to the ~~eighth~~ fourth task control block.

6. (currently amended): The real time control system of claim 1, wherein the operating system controls the ready queue so that switching between the tasks is achieved on a basis of the first priority link group, when task searching in the digital signal processor is based on an order of the priority of the tasks, and

controls the ready queue so that switching between the tasks is achieved on a basis of the ready queue link, when the task searching is based on a first-in first-out (FIFO) system.

7. (previously presented): The real time control system of claim 1, further comprising a timer wheel for managing timer control blocks for the tasks in a pointer arrangement structure, wherein the operating system inserts the timer control blocks into corresponding slots of the timer wheel according to a time set for the tasks in the digital signal processor.

8. (previously presented): The real time control system of claim 7, wherein the timer wheel is divided into two timer wheels according to a predetermined reference time, and the operating system inserts timer control blocks corresponding to slots of the first timer wheel when the time set for the tasks is equal to or less than the predetermined reference time, and inserts timer control blocks corresponding to slots of the second timer wheel when the time set for the

tasks is greater than the predetermined reference time and equal to or less than twice the predetermined reference time.

9. (previously presented): The real time control system of claim 8, wherein the operating system generates errors when the time set for the tasks is greater than twice the predetermined reference time.

10. (previously presented): The real time control system of claim 1, wherein a memory used to process the tasks in the digital signal processor is divided into an internal memory and an external memory in the digital signal processor, and the operating system manages the internal memory and the external memory using a memory structure made up of a start address, an end address, a memory size, a memory map, and next information indicating the start address of a next memory to be connected.

11. (original): The real time control system of claim 10, wherein the operating system manages the memory so that the internal memory is allocated when the digital signal processor is required to perform fast processing on a task, and so that the external memory is allocated when the internal memory is completely allocated.

12. (original): The real time control system of claim 10, wherein the operating system manages the memory so that the external memory is divided into a plurality of memories using the memory structure.

13. (previously presented): The real time control system of claim 10, wherein the operating system allocates and returns the memory in units of predetermined-sized pages in a system call way, and checks allocation or non-allocation of the memory on the basis of the map of a memory.